3D System Integration

An Interconnect Hierarchy driven Technology Landscape

Eric Beyne, imec

It is becoming increasingly clear that 3D integration complements semiconductor scaling in enabling higher integration density as well as heterogeneous technology integration. Using 3D technology, it is possible to extend the number of functions per 3D chip well beyond the capabilities of traditional scaling. In addition, one can combine a wide variety of device technologies to optimize system performance.

The field of 3D integration has been very active over the past ten years. A large number of technology directions have been proposed and many different names and acronyms have been created to identify different technologies. Unfortunately this also often created confusion for those trying to compare and select technologies for system applications. In this presentation, A hierarchical view on the need for 3D interconnects will be presented, offering a landscape view on technology options, from relatively coarse package level 3D integration technologies to ultra-dense sub-micron transistor level stacking technologies. Examples will be shown and possible technology directions will be given.